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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,275	01/23/2002	Franco Motika	POU920000057US1	6761

7590 02/24/2005

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

Lynn L. Augspurger
IBM Corporation
2455 South Road, P386
Poughkeepsie, NY 12601

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,275	MOTIKA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 10-13* is/are allowed.

6)☒ Claim(s) *8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. In view of the amendment filed 11/26/2004, all objections to the drawing are withdrawn.

Specification

2. In view of the amendment filed 11/26/2004, all objections to the abstract are withdrawn.

Claim Rejections - 35 USC § 112

3. Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The preamble in claim 8 recites, "A method of testing an integrated circuit". The omitted elements are: necessary elements or relationships relating claim limitation b and c to method steps (Note: claim limitation b and c are not method steps but recite specific components of an integrated circuit).

Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites, "on a shift register latch by shift register latch basis", which is incomprehensible.

Response to Arguments

4. Applicant's arguments with respect to claims 8 and 9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger; Edward B. et al. (US 4687988 A, hereafter referred to as Eichelberger) in view of Koenemann; Bernd K. F. et al. (US 5612963 A, hereafter referred to as Koenemann).

35 U.S.C. 103(a) rejection of claim 8.

Eichelberger teaches a pseudo random pattern generator for generating at least one flat pseudo random pattern (LFSR 100 in Figure 1 and 2 of Eichelberger is a pseudo random pattern generator for generating at least one flat pseudo random pattern; Note: an LFSR generates test patterns substantially with as many zeros as ones, hence is a flat pseudo random pattern generator having no weight); weighting circuits for providing a selectable weight set to said flat pseudo random patterns (Weighting Circuit 300 in Figure 3 and 300-1 to 300-96 in Figure 4 of Eichelberger teaches weighting circuits for providing a selectable weight set to said flat pseudo random patterns; col. 8, lines 13-53 in Eichelberger teaches that the weighting set comprises {0, ¼, 1/3, ½, 1}); a storage element associated with each of the weighting pattern generators receipt of a random pattern from the associated random pattern generator (Col 10, lines 34-43 in Eichelberger teaches an LSSD shift register storage element for each of the inputs of DUT 50 in Figure 4 of Eichelberger associated with each of the weighting pattern generators receipt of a random pattern from the associated weighted random pattern generator 300-1 to 300-96); and a selection circuit for individually addressing each of the storage elements for providing said weighted pseudo random pattern to said scan chains independently of one another for scanning said weighted pattern to said logic circuits to enable provision of different weights to the storage elements (each of the weighted random pattern generator 300-1 to 300-96 has a selection circuit MPX 305 in Figure 3 for individually addressing each of the LSSD shift register storage elements for

each of the inputs of DUT 50 in Figure 4 of Eichelberger for providing said weighted pseudo random pattern to said LSSD scan chains independently of one another for scanning said weighted pattern to said logic circuits to enable provision of different weights to the storage elements; Note: col. 2, lines 45-50 in Eichelberger teach that the weighting of the applied test patterns is a function of the number and kind of internal circuit elements that are directly or indirectly affected by an input signal on the respective input terminals of the device, hence the storage elements for providing said weighted pseudo random pattern to said scan chains are addressed independently of one another for scanning said weighted pattern to said logic circuits to enable provision of different weights to the storage elements since the weighting can depend only on the number and kind of internal circuit elements that are directly affected by an input signal on the respective input terminals of the device).

However Eichelberger does not explicitly teach the specific use of BIST technology whereby the Weighting circuitry 300-1 to 300-96 in Figure 4 of Eichelberger are part of the integrated circuit under test.

Koenemann, in an analogous art, teaches use of BIST technology whereby the Weighting circuitry are part of the integrated circuit under test (see col. 3, lines 1-3 and Figure 4 in Koenemann).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Eichelberger with the teachings of Koenemann by including use of BIST technology whereby the Weighting circuitry 300-1 to 300-96 in Figure 4 of Eichelberger are part of the integrated circuit under test. This modification

would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of BIST technology whereby the Weighting circuitry 300-1 to 300-96 in Figure 4 of Eichelberger are part of the integrated circuit under test would have provided the opportunity to allow for self-testing.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133